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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)	
JRL-550-466	

Application Number	Filed
10/691,501	October 23, 2003
First Named Inventor	
FLYNN	
Art Unit	Examiner
2189	Dinh, Ngoc V.

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

☐ Applicant/Inventor

☐ Assignee of record of the entire interest. See 37 C.F.R. § 3.71. Statement under 37 C.F.R. § 3.73(b) is enclosed. (Form PTO/SB/96)

☒ Attorney or agent of record 33,149 (Reg. No.)

☐ Attorney or agent acting under 37CFR 1.34.
Registration number if acting under 37 C.F.R. § 1,34 _____

Signature

John R. Lastova
Typed or printed name

703-816-4025
Requester's telephone number

June 18, 2007
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.*

☒ *Total of 1 form/s are submitted.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

FLYNN et al — Atty. Ref.: 550-466; Confirmation No. 2384

Appl. No. 10/691,501 — TC/A.U. 2189

Filed: October 23, 2003 — Examiner: Dinh, Ngoc V.

For: HARDWARE DRIVEN STATE SAVE/RESTORE IN A DATA PROCESSING SYSTEM

* * * * * * * * * * *

June 18, 2007

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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Most of the claims stand rejected under 35 U.S.C. §102 for anticipation based on Godfrey. Because Godfrey does not disclose every feature recited in the independent claims, this rejection should be withdrawn.

Clear Error #1: Godfrey's System Bus 100 Is Not Coupled To the Memory 200

The independent claims require "a multi-bit wide system bus, coupled to said circuit and said memory, for transferring multi-bit data words between said circuit and said memory in response to memory transfer requests issued upon said system bus during normal processing operation of said circuit and said memory." Quoted from claim 1. The Examiner maps the claimed memory to the external memory 200 shown in Figure 2 of Godfrey and the claimed multi-bit wide system bus to the internal bus 100. Figure 2 reproduced here clearly shows that the internal bus 100 (the thickest black line) is not coupled or connected to the external memory

200. Only the SCAN_PATH[1] (the medium thickness black line) is connected to the external memory 200 and to the device state registers 104a, 108a, 112a, etc. The SCAN_PATH is not shown or described as connected to the internal bus 100. The internal bus 100 is only shown coupling the peripheral devices to each other and the execution unit 124.

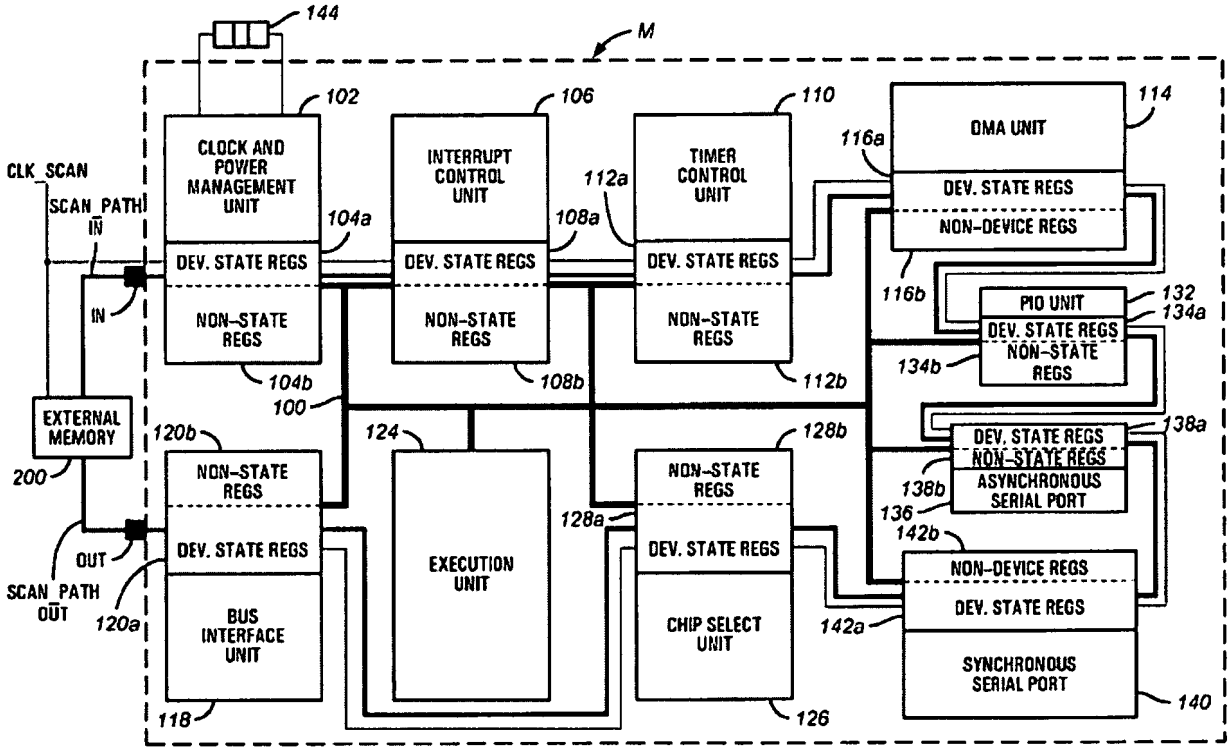

FIG. 2

The SCAN_PATH is clearly a separate path from the internal bus 100. A single configuration scan data out pin OUT is coupled to the external memory 4:65-67, and the configuration scan data from each peripheral is "sequentially shifted out of each configuration register into external memory 200 via SCAN_PATH." 4:67-5:2. Similarly, "the external memory 200 is coupled to the input pin IN, so that configuration scan data from external memory 200 can be synchronously shifted into each peripheral configuration register via

[1] The SCAN_PATH cannot be the claimed system bus that transfers multi-bit wide data words, meaning that multiple bits are transferred in parallel, because the one wire scan path transfers data serially. See e.g., 4:48-65.

SCAN_PATH." Col. 5, lines 3-6. Nor is there disclosure of the internal bus 100 being coupled to the SCAN_PATH.

Clear Error #2: Godfrey's System Bus 100 Does Not Transfer Multi-Bit Data Words Between The Circuit And The Memory 200

During normal operation, the internal bus 100 of Godfrey does not transfer multi-bit data words between the claimed circuit (the elements within the dotted line of Figure 2 labeled as the microcontroller M) and the external memory 200 in response to memory transfer requests issued upon the internal bus 100. The internal bus 100 communicates with the various peripherals and the execution unit shown as coupled to bus 100 in Figure 2, i.e., the elements within the dotted line. But this circuit M within the dotted lines does not include the external memory 200.

The Examiner makes reference to 3:65-4:5. Here, Godfrey states: "The microcontroller M preferably includes an internal bus 100 coupling a variety of functional units and registers (herein referred to as peripheral devices except the execution unit), used to control and monitor those units. These peripheral devices include a clock and power management unit 102 with corresponding clock/power registers 104." Nothing in this text teaches that Godfrey's internal system bus 100 transfers multi-bit data words between the circuit M defined by the dotted lines and the external memory 200 outside of the dotted line box.

The external memory 200 is only connected to the serial SCAN_PATH. Godfrey does not teach using the SCAN_PATH during normal processing operations. As noted above, the SCAN_PATH in Godfrey is a single bit-wide data path and does not transfer multi-bit data words. The Examiner references 5:22-25 and 8:12, 13, 34, and 35. 5:22-25 describes that a function of a UART peripheral to convert data between serial and parallel form. A UART is not relevant to the claims. 8:12, 13, 34, and 35 relate to parallel transfer between state register stages and registers. But the question is what is the bus width of the scan data communicated

between the microcontroller M and the external memory 200. The answer is single bit (serial) and not multi-bit.

Clear Error #3: <u>Godfrey Does Not Transfer The State Information To/From Memory Using The Multi-Bit Wide System Bus.</u>

The independent claims also require:

> a state saving controller, coupled to said circuit and said system bus, configured in response to a state saving trigger to read said data values defining a state of said circuit from said one or more nodes and to generate a sequence of memory write requests on said system bus that write one or more state saving multi-bit data words representing said data values into said memory such that said state of said circuit is restorable using said one or more state saving multi-bit data words.

Quoted from claim 1. The Examiner maps the state saving controller onto the microcontroller M which applies a trigger to the state registers. The Examiner refers to 8:54-60 as discussing the use of the system bus for 100 writing one or more state saving multi-bit data words into the external memory 200. But it is the serial SCAN_PATH coupled to the external memory 200 that takes signal values from the configuration registers and saves them in the external memory 200 or loads them back from the external memory 200. These writes to and reads from the external memory 200 do not take place using the multi-bit wide system bus 100.

The independent claim technology reuses the system bus and the memory to provide state saving functionality with speed and efficiency. Godfrey's single bit wide serial scan chain is significantly slower than a multi-bit wide system bus in performing such state saving and restore operations. Furthermore, the serial scan chain of Godfrey is a separate structure provided, at least partially, for this purpose and is not used during normal processing operations. Consequently, Godfrey's serial scan chain is an additional circuit overhead.

Given the clear errors set forth above, the final rejection should be withdrawn, and the application passed to allowance.

Respectfully submitted,

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